

CLAIMS

1. An integrated circuit on a substrate, comprising:

a first well having a first dopant concentration and including a second

5 conductivity low-voltage transistor;

a second well having a dopant concentration equal to the first dopant concentration and including a first conductivity high-voltage transistor;

a third well having a second dopant concentration of an opposite type than the first well and including a first conductivity low-voltage transistor; and

10 wherein the first conductivity low-voltage transistor and the second conductivity low-voltage transistor are created without a threshold voltage (V_t) implant.

2. The integrated circuit of claim 1, wherein the first conductivity high-voltage transistor is a lateral dual-diffusion metal oxide semiconductor.

3. The integrated circuit of claim 2, wherein the first conductivity high-voltage transistor has a breakdown voltage of greater than 40 volts.

20 4. The integrated circuit of claim 1, further comprising an energy dissipation element coupled to said first conductivity high-voltage transistor.

5. A fluid jet printhead, comprising:

the integrated circuit of claim 4; and

25 an orifice layer defining an opening for ejecting fluid thermally coupled to said energy dissipation element, said orifice layer disposed on the surface of the integrated circuit.

6. A recording cartridge, comprising:

30 the fluid jet printhead of claim 5;

a body defining a fluid reservoir, said fluid reservoir fluidically coupled to the opening in said orifice layer of the fluid jet printhead; and

a pressure regulator to control the pressure of the fluid reservoir within the body of the recording cartridge.

7. A recording device for placing fluid on a medium, comprising:

- 5 the recording cartridge of claim 6; and
 a transport mechanism to move the recording cartridge in at least one direction with respect to the medium.

8. The integrated circuit of claim 1 wherein the first and second wells are an N-wells
 10 and wherein the third well is a P-well.

9. The integrated circuit of claim 1 wherein the first conductivity high-voltage transistor is an n conductivity high-voltage transistor.

15 10. A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, comprising the steps of:

 creating a defined deposition of a first dielectric layer to expose a first region and a second region; then consisting essentially of the steps of:

- 20 implanting a first conductivity dopant into the first and second regions;
 applying a first protective coating over the first and second regions;
 driving in the first conductivity dopant into the substrate;
 removing the first dielectric layer;
 creating a defined deposition of a second dielectric layer in the same location
 25 as the defined deposition of the first dielectric layer;
 implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer;
 driving in the second conductivity dopant into the substrate;
 removing the first protective coating and the second dielectric layer;

creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor;

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor;

applying a second protective coating over the first and second regions;

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor;

removing the second protective coating;

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located;

removing the patterned third dielectric layer; and

then further comprising the steps of:

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

11. An integrated circuit made by the process of claim 10.

12. A method of creating an integrated circuit having a second conductivity low-voltage transistor in a first region, a first conductivity high-voltage transistor in a second region, and a first conductivity low-voltage transistor in a third region, comprising the steps of:

doping the first and second regions with a first dopant concentration to control the threshold voltage of the second conductivity low-voltage transistor; and

doping the third region with a second dopant concentration to control the threshold voltage of the first conductivity low-voltage transistor;

wherein a voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed.

13. An integrated circuit made by the process of claim 12.

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14. A method of processing an integrated circuit having a second conductivity low-voltage transistor in a first region, a first conductivity high-voltage transistor in a third region, and a first conductivity low-voltage transistor in a second region, comprising the steps of:

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doping the first and second regions with a first dopant concentration; and

doping the third region with a second dopant concentration; and

excluding the step of:

implanting a threshold voltage adjustment of the first and second low-voltage transistors and

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wherein the first and second regions have the substantially the same dopant concentration after processing of the integrated circuit.

15. An integrated circuit made by the process of claim 14.

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16. A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, comprising the steps of:

creating a defined deposition of a first dielectric layer to expose a first region and a second region; then

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implanting a first conductivity dopant into the first and second regions; then

applying a first protective coating over the first and second regions; then

driving in the first conductivity dopant into the substrate; then

removing the first dielectric layer; then

creating a defined deposition of a second dielectric layer in the same location

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as the defined deposition of the first dielectric layer; then

implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer; then

driving in the second conductivity dopant into the substrate; then

removing the first protective coating and the second dielectric layer; then

5 creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor; then

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor; then

10 applying a second protective coating over the first and second regions; then

implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor; then

removing the second protective coating; then

15 creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located; then

removing the patterned third dielectric layer;

creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;

depositing a gate material over the sixth dielectric layer; and

20 patterning the sixth dielectric layer and the gate material to define gate regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

17. An integrated circuit made by the process of claim 16.